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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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FOLEY AND LARDNER
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WASHINGTON, DC 20007

EXAMINER

PIZIALI, JEFFREY J

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/609,384

Applicant(s)

KODATE ET AL.

Examiner

Jeff Piziali

Art Unit

2673

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>01 July 2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figure 14 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see Page 7, Lines 6-8 of the Specification). See MPEP § 608.02(g).
Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The disclosure is objected to because of the following informalities: On Page 2, Line 7, "decreases" should be changed to "decrease." Appropriate correction is required.

Information Disclosure Statement

4. The listing of references in the specification is not a proper information disclosure statement (see Page 28, Lines 14-17 of the Specification). 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609 A(1) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Sakamoto (US 6,028,577 A).

Regarding claim 1, Sakamoto discloses an image display element [Figs. 7 & 10A; 1] comprising: a plurality of data lines [Figs. 7 & 10A; 3] that supply display signals; a plurality of scan lines [Figs. 7 & 10A; 2] that supply scan signals; a first pixel electrode [Figs. 7 & 10A; 1(i, j)] and a second pixel electrode [Figs. 7 & 10A; 1(i+1, j)] that are supplied with display signals from one data line [Figs. 7 & 10A; 3(j)] (see Column 11, Lines 35-61); a first electrostatic shielding unit [Fig. 7; 7a (left side)] that shields the first pixel electrode from an electric field produced by a data line that is adjacent to the first pixel electrode; and a second electrostatic

shielding unit [Fig. 7; 7a (right side)] that shields the second pixel electrode from an electric field produced by a data line that is adjacent to the second pixel electrode (see Column 13, Lines 17-52).

Regarding claim 2, Sakamoto discloses a first switching device [Fig. 10B; 6(i, j)] that controls a supply of the display signal in the one data line, wherein the first switching device is electrically connected between the one data line and the first pixel electrode and has a gate electrode; a second switching device [Fig. 10B; 6(i, j-1)] that is electrically connected between the gate electrode of the first switching device and a predetermined scan line; and a third switching device [Fig. 10B; 6(i+1, j)] that is connected to the one data line and that controls a supply of the display signal to the second pixel electrode (see Column 11, Line 62 - Column 12, Line 67).

Regarding claim 3, Sakamoto discloses the first electrostatic shielding unit is formed by a first conductive layer [Fig. 8; 7a (left side)] that is disposed adjacent to the data line in a lower layer than the first pixel electrode [Fig. 8; 1(i, j)], and the second electrostatic shielding unit is formed by a second conductive layer [Fig. 8; 7a (right side)] that is disposed adjacent to the data line in the lower layer than the second pixel electrode [Fig. 8; 1(i+1, j)] (see Column 13, Lines 55-59).

Regarding claim 4, Sakamoto discloses the first electrostatic shielding unit [Fig. 8; 7a (left side)] and the first pixel electrode [Fig. 8; 1(i, j)] have areas that are partially superimposed

with each other in a direction that is perpendicular to the surface of layers, and the second electrostatic shielding unit [Fig. 8; 7a (right side)] and the second pixel electrode [Fig. 8; 1(i+1, j)] have areas that are partially superimposed with each other in the direction that is perpendicular to the surface of layers (see Column 13, Lines 55-59).

Regarding claim 5, Sakamoto discloses a first capacitor line [Figs. 7 & 10B; C2] that is disposed in an area partially superimposed with the first pixel electrode in the direction that is perpendicular to the surface of layers in the peripheral lower layer of the first pixel electrode facing the area in which the first electrostatic shielding unit is disposed, and that is connected to the first electrostatic shielding unit; and a second capacitor line [Figs. 7 & 10B; C1] that is disposed in an area partially superimposed with the second pixel electrode in the direction that is perpendicular to the surface of layers in the peripheral lower layer of the second pixel electrode facing the area in which the second electrostatic shielding unit is disposed, and that is connected to the second electrostatic shielding unit (see Column 13, Line 65 - Column 14, Line 6).

Regarding claim 6, Sakamoto discloses the first electrostatic shielding unit and the second electrostatic shielding unit are electrically connected to each other (see Fig. 7; Column 13, Lines 17-28).

Regarding claim 7, Sakamoto discloses the first electrostatic shielding unit and the second electrostatic shielding unit are electrically connected to a wiring structure that has a predetermined potential (see Fig. 7; Column 13, Lines 17-59).

Regarding claim 8, Sakamoto discloses the first electrostatic shielding unit and the second electrostatic shielding unit are connected to a predetermined scan line [Fig. 7; 2(i)] (see Column 13, Lines 17-59).

Regarding claim 9, Sakamoto discloses the first electrostatic shielding unit and the second electrostatic shielding unit are connected to a potential supply line that has a predetermined potential (see Fig. 7; Column 13, Lines 17-59).

Regarding claim 10, Sakamoto discloses the predetermined potential is maintained within a range of a potential variation of the pixel electrode (see Fig. 7; Column 13, Lines 17-59).

Regarding claim 11, Sakamoto discloses the predetermined potential is maintained within a range of a potential variation of a common electrode [Fig. 7; 7b] that is disposed on a counter substrate disposed opposite to a substrate on which the pixel electrode is disposed with a predetermined distance between the substrates (see Column 13, Lines 17-59).

Regarding claim 12, this claim is rejected by the reasoning applied in rejecting claim 1; furthermore, Sakamoto discloses a data line driving circuit [Fig. 10A; 5] and a scan line driving circuit [Fig. 10; 4] (see Column 11, Lines 35-58).

Regarding claim 13, this claim is rejected by the reasoning applied in rejecting claim 2.

Regarding claim 14, this claim is rejected by the reasoning applied in rejecting claim 8.

Regarding claim 15, this claim is rejected by the reasoning applied in rejecting claim 9.

Regarding claim 16, this claim is rejected by the reasoning applied in rejecting claim 10.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hebiguchi (US 6,292,237 B1), Sasano et al (US 5,671,027 A), Kitajima et al (US 5,475,396 A), Kanemori et al (US 5,434,686 A), Oki et al (US 5,408,252 A), Atsumi et al (US 5,337,173 A), Wu (US 5,193,018 A), Kabuto et al (US 5,151,689 A), Shannon (US 4,931,787 A), Noguchi (US 4,781,438 A), Saito (US 4,775,861 A), and Morozumi (US 4,600,274 A) are cited to further evidence the state of the art pertaining to image display elements.

Art Unit: 2673

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Piziali whose telephone number is (571) 272-7678. The examiner can normally be reached on Monday - Friday (6:30AM - 3PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



J.P.

3 August 2005



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